In the Claims:

Claim 1-28 (canceled).

Claim 29 (new): A processor comprising:

a first thread and a second thread, said first thread comprising a first processing unit and said second thread comprising a second processing unit;

a first instruction packet and a second instruction packet, said first instruction packet comprising at most two issue groups and said second instruction packet comprising at most two issue groups, each of said at most two issue groups of said first instruction packet and each of said at most two issue groups of said second instruction packet comprising at most 64 bits and requiring an internal instruction bus no greater than 64 bits wide for transport to one of said first and second processing units;

each of said first and second threads receiving a respective one of said at most two issue groups of a respective one of said first and second instruction packets;

said first processing unit executing one of said at most two issue groups of said first instruction packet and said second processing unit executing one of said at most two issue groups of said second instruction packet in a single clock cycle;

each of said at most two issue groups of each of said first and second instruction packets performing an operation on data fetched from an exclusive thread memory communicating with only one of said first and second threads, a

result of said operation being stored back in said exclusive thread memory communicating with said only one of said first and second threads.

Claim 30 (new): The processor of claim 29 wherein said each of said first and second instruction packets is 128 bits wide.

Claim 31 (new): The processor of claim 29 wherein said first instruction packet comprises two issue groups, wherein a first one of said two issue groups is 64 bits wide and a second one of said two issue groups is 48 bits wide.

Claim 32 (new): The processor of claim 29 wherein said first instruction packet comprises two issue groups, wherein a first one of said two issue groups is 48 bits wide and a second one of said two issue groups is 64 bits wide.

Claim 33 (new): The processor of claim 29 wherein said each of said first and second instruction packets resides in a respective instruction cache and is addressed by a respective program counter.

Claim 34 (new): A method for improving performance of a VLIW processor comprising:

dividing a first instruction packet into first and second issue groups, each of said first and second issue groups of said first instruction packet comprising at most 64 bits;

dividing a second instruction packet into first and second issue groups, each of said first and second issue groups of said second instruction packet comprising at most 64 bits;

providing, through a first internal instruction bus no greater than 64 bits wide, said first issue group of said first instruction packet to a first thread having a first thread processing unit and, through a second internal instruction bus no greater than 64 bits wide, said first issue group of said second instruction packet to a second thread having a second thread processing unit during a first clock cycle; and

providing, through said first internal instruction bus, said second issue group of said first instruction packet to said first thread having said first thread processing unit and, through said second internal instruction bus, said second issue group of said second instruction packet to said second thread having said second thread processing unit during a second clock cycle, wherein said first instruction packet is a different instruction packet than said second instruction packet;

fetching data from an exclusive thread memory communicating with only one of said first and second threads;

performing an operation on said data by one of said first and second issue groups of said first instruction packet and said first and second issue groups of said second instruction packet;

storing back a result of said operation in said exclusive thread memory communicating with said only one of said first and second threads.

Claim 35 (new): The method of claim 34 wherein each of said first and second instruction packets consists of 128 bits.

Claim 36 (new): The method of claim 34 wherein said first issue group of said first instruction packet comprises 64 bits and said second issue group of said first instruction packet comprises 48 bits.

Claim 37 (new): The method of claim 34 wherein said first issue group of said first instruction packet comprises 48 bits and said second issue group of said first instruction packet comprises 64 bits.

Claim 38 (new): The method of claim 34 wherein said first issue group of said second packet comprises 64 bits and said second issue group of said second packet comprises 48 bits.

Claim 39 (new): The method of claim 34 wherein said first issue group of said second packet comprises 48 bits and said second issue group of said second packet comprises 64 bits.

Claim 40 (new): A method for improving performance of a VLIW processor comprising:

dividing a first instruction packet into first and second issue groups and a second instruction packet into first and second issue groups, each of said first and second issue groups of said first instruction packet and said first and second issue groups of said second instruction packet comprising at most 64 bits;

providing each of said first and second issue groups of said first instruction packet and said first and second issue groups of said second instruction packet, in one of two clock cycles, to a respective thread having a respective processing unit, said each of said first and second issue groups of said first instruction packet and said first and second issue groups of said second instruction packet requiring an internal instruction bus no greater than 64 bits wide for transport to said respective processing unit;

executing said first and second instruction packets in said two clock cycles, wherein an issue group from each of said first and second instruction packets is executed in one of said two clock cycles;

fetching data from an exclusive thread memory communicating with only one thread;

performing an operation on said data by one of said first and second issue groups of said first instruction packet and said first and second issue groups of said second instruction packet;

storing back a result of said operation in said exclusive thread memory communicating with said only one thread.

Claim 41 (new): The method of claim 40 wherein said each of said first and second instruction packets is 128 bits wide.

Claim 42 (new): The method of claim 40 wherein said first issue group of said first instruction packet is 64 bits wide and said second issue group of said first instruction packet is 48 bits wide.

Claim 43 (new): The method of claim 40 wherein said first issue group of said first instruction packet is 48 bits wide and said second issue group of said first instruction packet is 64 bits wide.

Claim 44 (new): The method of claim 40 wherein said first issue group of said second instruction packet is 64 bits wide and said second issue group of said second instruction packet is 48 bits wide.

Claim 45 (new): The method of claim 40 wherein said first issue group of said second instruction packet is 48 bits wide and said second issue group of said second instruction packet is 64 bits wide.

Claim 46 (new): The method of claim 40 wherein said each of said first and second instruction packet resides in a respective instruction cache and is addressed by a respective program counter.